

This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

**As rescanning documents *will not* correct images,
please do not report the images to the
Image Problems Mailbox.**

DIALOG(R)File 345:Inpadoc/Fam.& Legal Stat

(c) 2003 EPO. All rts. reserv.

-13823653

Basic Patent (No,Kind,Date): JP 9186336 A2 970715 <No. of Patents: 001>

METHOD OF MANUFACTURING THIN FILM TRANSISTOR (English)

Patent Assignee: CASIO COMPUTER CO LTD

Author (Inventor): KUDO TOSHIO; WAKAI HARUO

IPC: *H01L-029/786; H01L-021/336

CA Abstract No: 127(13)184293T

Language of Document: Japanese

Patent Family:

Patent No	Kind	Date	Applic No	Kind	Date
JP 9186336	A2	970715	JP 95351234	A	951227 (BASIC)

Priority Data (No,Kind,Date):

JP 95351234 A 951227

DIALOG(R)File 347:JAPIO

(c) 2003 JPO & JAPIO. All rts. reserv.

05571536 **Image available**

METHOD OF MANUFACTURING THIN FILM TRANSISTOR

PUB. NO.: 09-186336 [JP 9186336 A]

PUBLISHED: July 15, 1997 (19970715)

INVENTOR(s): KUDO TOSHIO

 WAKAI HARUO

APPLICANT(s): CASIO COMPUT CO LTD [350750] (A Japanese Company or
 Corporation), JP (Japan)

APPL. NO.: 07-351234 [JP 95351234]

FILED: December 27, 1995 (19951227)

INTL CLASS: [6] H01L-029/786; H01L-021/336

JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)

JAPIO KEYWORD: R002 (LASERS); R004 (PLASMA); R096 (ELECTRONIC MATERIALS --
 Glass Conductors)

ABSTRACT

PROBLEM TO BE SOLVED: To simplify the bottom gate type polysilicon thin film transistor.

SOLUTION: A hydrogen containing true amorphous silicon thin film 25 and a channel protective film forming film 26 comprising a silicon nitride are continuously formed on the surface of the second insulating film 24. Next, the amorphous silicon film 25 is dehydrogenated by irradiating the film 25 with excimer laser in low density in the atmosphere and then the true amorphous silicon thin film 25 is polymerized to form a true polysilicon thin film 27. At this time, this step can be performed simply by changing the energy density of the excimer laser. Besides, after the formation of a channel protective film 26a, a source region 28a and a drain region 28b are formed of a formed n type silicon film. In such a case, both impurity implanting step and activating step can be eliminated.

(19) 日本国特許庁 (J P)

(12) 公開特許公報 (A)

(11) 特許出願公開番号

特開平9-186336

(43) 公開日 平成9年(1997)7月15日

(51) Int.Cl.⁶

H 0 1 L 29/786

21/336

識別記号

庁内整理番号

F I

H 0 1 L 29/78

技術表示箇所

6 2 7 E

6 2 7 G

審査請求 未請求 請求項の数 6 F D (全 6 頁)

(21) 出願番号 特願平7-351234

(22) 出願日 平成7年(1995)12月27日

(71) 出願人 000001443

カシオ計算機株式会社

東京都新宿区西新宿2丁目6番1号

(72) 発明者 工藤 利雄

東京都八王子市石川町2951番地の5 カシ
オ計算機株式会社八王子研究所内

(72) 発明者 若井 晴夫

東京都八王子市石川町2951番地の5 カシ
オ計算機株式会社八王子研究所内

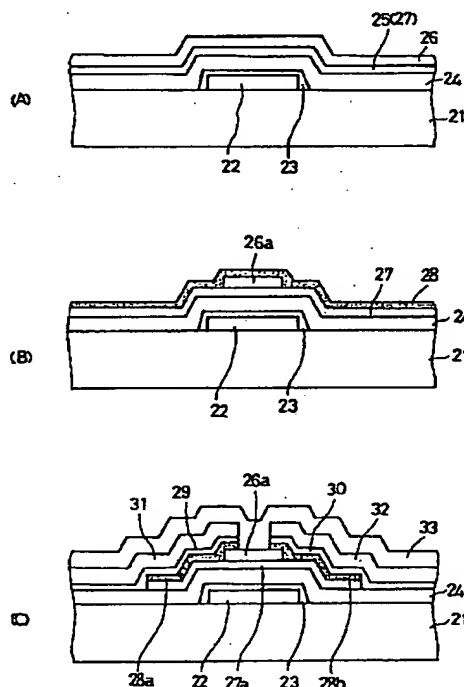
(74) 代理人 弁理士 杉村 次郎

(54) 【発明の名称】 薄膜トランジスタの製造方法

(57) 【要約】

【課題】 ボトムゲート型のポリシリコン薄膜トランジスタの製造工程を簡略化する。

【解決手段】 第2ゲート絶縁膜24の上面に水素含有の真性なアモルファスシリコン薄膜25および窒化シリコンからなるチャネル保護膜形成用膜26を連続して成膜する。次に、大気中においてエキシマレーザを低エネルギー密度で照射することにより、アモルファスシリコン薄膜25の脱水素化処理を行い、次いで同じく大気中においてエキシマレーザを高エネルギー密度で照射することにより、真性なアモルファスシリコン薄膜25をポリ化して真性なポリシリコン薄膜27を形成する。この場合、エキシマレーザのエネルギー密度を変えるだけでよい。また、チャネル保護膜26aを形成した後、ソース領域28aおよびドレイン領域28bを、成膜したn型シリコン膜によって形成する。この場合、不純物注入工程および活性化工程が不要となる。



【特許請求の範囲】

【請求項1】 ソース、ドレイン、チャネル領域を有するポリシリコンを活性半導体層とする薄膜トランジスタの製造方法において、水素化アモルファスシリコン膜に、エキシマレーザを前回の照射領域と50%以上オーバーラップさせて照射するスキャン走査を全領域に行つて、前記水素化アモルファスシリコン膜を脱水素化およびポリ化することを特徴とする薄膜トランジスタの製造方法。

【請求項2】 請求項1記載の発明において、エキシマレーザを前回と90%以上オーバーラップさせることを特徴とする薄膜トランジスタの製造方法。

【請求項3】 請求項1記載の発明において、エキシマレーザを短い幅を有する細長い帯状のビーム形状とし、この帯状ビームの幅方向にスキャン走査することを特徴とする薄膜トランジスタの製造方法。

【請求項4】 請求項1記載の発明において、エキシマレーザを複数回照射した上、スキャン走査することを特徴とする薄膜トランジスタの製造方法。

【請求項5】 請求項4記載の発明において、前記複数回のエキシマレーザの照射は最初が最もエネルギー密度が低いことを特徴とする薄膜トランジスタの製造方法。

【請求項6】 請求項1記載の発明において、全領域をスキャン走査後、1回目よりもエネルギー密度を大きくして再度エキシマレーザを照射しながらスキャン走査することを特徴とする薄膜トランジスタの製造方法。

【発明の詳細な説明】**【0001】**

【発明の属する技術分野】この発明は薄膜トランジスタの製造方法に関し、特にボトムゲート型のポリシリコン薄膜トランジスタの製造方法に関する。

【0002】

【従来の技術】図3は従来のボトムゲート型のポリシリコン薄膜トランジスタの製造工程を示し、図4(A)～(D)はそれぞれ図3に示す製造工程を経て製造される薄膜トランジスタの各状態における断面図を示したものである。この薄膜トランジスタの製造に際しては、まず図3に示すゲート電極形成工程Aにおいて、図4(A)に示すように、ガラス基板1の上面の所定の個所にゲート電極2を形成する。次に、図3に示す2層連続成膜工程Bにおいて、ゲート電極2を含むガラス基板1の上面全体にゲート絶縁膜3および水素含有の真性なアモルファスシリコン薄膜4を連続して成膜する。次に、図3に示す脱水素化工程Cにおいて、後の工程でエキシマレーザ照射により高エネルギーを与えたとき水素が突沸して欠陥が生じるのを避けるために、脱水素化用電気炉で熱処理を行うことにより、アモルファスシリコン薄膜4中の水素濃度を低減する。

【0003】次に、図3示すポリ化工程Dにおいて、エキシマレーザを高エネルギー密度で照射することにより、

真性なアモルファスシリコン薄膜4をポリ化して真性なポリシリコン薄膜5を形成する。次に、図3に示す不純物注入工程Eにおいて、図4(B)に示すように、ポリシリコン薄膜5のうちチャネル領域5aとなる領域上に不純物注入マスク6を形成し、ポリシリコン薄膜5のうちチャネル領域5aを除く全領域にリン等のn型不純物を注入する。この後、不純物注入マスク6を剥離する。次に、図3に示す活性化工程Fにおいて、エキシマレーザを低エネルギー密度で照射することにより、n型不純物注入領域を活性化する。次に、図3に示すチャネル保護膜形成工程Gにおいて、図4(C)に示すように、ポリシリコン薄膜5のうちチャネル領域5aとなる領域上にチャネル保護膜7を形成する。

【0004】次に、図3に示すデバイスエリア形成工程Hにおいて、図4(D)に示すように、ポリシリコン薄膜5のうち不要な部分を除去する。この状態では、ポリシリコン薄膜5の中央部は真性領域からなるチャネル領域5aとされ、その両側はn型不純物注入領域からなるソース領域5bおよびドレイン領域5cとされている。次に、図3に示すソース・ドレイン電極形成工程Iにおいて、チャネル保護膜7の上面両側およびソース領域5b、ドレイン領域5cの各上面等にソース電極8およびドレイン電極9を形成する。次に、図3に示すオーバーコート膜成膜工程Jにおいて、全上面にオーバーコート膜10を成膜する。次に、図3に示す水素化工程Kにおいて、水素化用電気炉または水素化用プラズマ炉で水素化処理を行うことにより、ポリシリコン薄膜5のダングリングボンドを減少させる。かくして、ボトムゲート型のポリシリコン薄膜トランジスタが製造される。

【発明が解決しようとする課題】

【0005】ところで、従来のこのようなボトムゲート型のポリシリコン薄膜トランジスタの製造方法では、従来の同型のつまりボトムゲート型のアモルファスシリコン薄膜トランジスタの製造方法と比較すると、脱水素化工程C、ポリ化工程D、不純物注入工程E、活性化工程Fおよび水素化工程Kが付加されており、製造工程が複雑であるという問題があった。この場合、特に、脱水素化工程Cのための脱水素化用電気炉とポリ化工程Dおよび活性化工程Fのためのエキシマレーザ装置とが別々の装置であるので、製造工程が複雑となり、また設備投資が増大する要因となっている。この発明の課題は、製造工程を簡略化するとともに設備投資を低減化することである。

【0006】

【課題を解決するための手段】この発明は、ソース、ドレイン、チャネル領域を有するポリシリコンを活性半導体層とする薄膜トランジスタの製造方法において、水素化アモルファスシリコン膜に、エキシマレーザを前回の照射領域と50%以上オーバーラップさせて照射するスキャン走査を全領域に行つて、前記水素化アモルファス

シリコン膜を脱水素化およびポリ化するようにしたものである。

【0007】この発明によれば、水素化アモルファスシリコン膜に、エキシマレーザを前回の照射領域と50%以上オーバーラップさせて照射するスキャン走査によって、脱水素化工程とポリ化工程とを一度に行うことができることとなり、したがって製造工程を簡略化することができる、またこれに伴い設備投資を低減化することができる。

【0008】

【発明の実施の形態】図1はこの発明の一実施形態におけるボトムゲート型のポリシリコン薄膜トランジスタの製造工程を示し、図2(A)～(C)はそれぞれ図1に示す製造工程を経て製造される薄膜トランジスタの各状態における断面図を示したものである。この薄膜トランジスタの製造に際しては、まず図1に示すゲート電極形成工程Aにおいて、図2(A)に示すように、ガラス基板21の上面の所定の個所にアルミニウム-チタン合金からなるゲート電極22を形成する。次に、図1に示す陽極酸化工程Bにおいて、陽極酸化処理を行うことにより、ゲート電極22の表面に酸化アルミニウムからなる第1ゲート絶縁膜23を形成する。次に、図1に示す3層連続成膜工程Cにおいて、第1ゲート絶縁膜23を含むガラス基板21の上面全体に、PE-CVDにより、窒化シリコンからなる第2ゲート絶縁膜24、水素含有の真性なアモルファスシリコン薄膜25および窒化シリコンからなるチャネル保護膜形成用膜26を連続して成膜する。

【0009】次に、図1に示す脱水素化・ポリ化工程Dについて説明するが、この場合、水素含有の真性アモルファスシリコン薄膜25上にチャネル保護膜形成用膜26を成膜しているため、大気中において低エネルギー密度のエキシマレーザの照射により、水素含有の真性アモルファスシリコン薄膜25の脱水素化処理を行うことができる。そこで、まず大気中においてエキシマレーザを低エネルギー密度で例えば $60\sim 150\text{ mJ/cm}^2$ 程度で照射すると、アモルファスシリコン薄膜25中の水素濃度が低減し、次いで同じく大気中においてエキシマレーザを高エネルギー密度で例えば $150\sim 300\text{ mJ/cm}^2$ 程度で照射すると、真性なアモルファスシリコン薄膜25がポリ化して真性なポリシリコン薄膜27が形成される。このように、脱水素化工程とポリ化工程とをエキシマレーザのエネルギー密度を変えるだけで連続して行うことができるので、製造工程を簡略化することができる。

【0010】ところで、脱水素化・ポリ化工程Dにおけるエキシマレーザの照射は、ビームサイズを短い幅を有する細長い帯状とされたレーザビームをビームサイズの幅方向にオーバーラップさせながらスキャン照射することにより行う。この場合、オーバーラップ量を好ましく

は50%以上、より好ましくは90～99%とすることが重要である。また、エキシマレーザの照射は、低エネルギー密度と高エネルギー密度とを2回以上、好ましくは低エネルギー密度からエネルギー密度を除々に高くして、例えば $10\sim 20\text{ mJ/cm}^2$ 程度ずつ高くして、3回以上行うようにしてもよい。スキャン走査の方法としては、1領域においてエネルギー密度を除々に高くして複数回エキシマレーザを照射した後、この1領域と50%以上オーバーラップするようにシフトしてエキシマレーザの照射を行うスキャン走査を全領域に亘って繰り返す方法と、スキャン走査によって全領域に亘って低エネルギー密度でエキシマレーザを照射した上、エネルギー密度を大きくして再度エキシマレーザを全領域に照射する方法とがある。なお、エキシマレーザ照射の代わりに、ランプ照射を行うようにしてもよい。

【0011】次に、図1に示すチャネル保護膜形成工程Eにおいて、図2(B)に示すように、チャネル保護膜形成用膜26のうち不要な部分を除去することにより、ポリシリコン薄膜27上の所定の個所にチャネル保護膜26aを形成する。次に、図1に示すn型シリコン成膜工程Fにおいて、チャネル保護膜26aを含むポリシリコン薄膜27の上面全体にPE-CVDによりリン等がドーパされたn型シリコン膜28を成膜する。次に、図1に示すデバイスエリア形成工程Gにおいて、図2(C)に示すように、n型シリコン膜28のうち不要な部分を除去してソース領域28aおよびドレイン領域28bを形成するとともに、ポリシリコン薄膜27のうち不要な部分を除去してチャネル領域27aを形成する。すなわち、チャネル保護膜26aの上面両側およびその両側におけるチャネル領域27aの各上面にソース領域28aおよびドレイン領域28bを形成する。この場合、チャネル領域27aは真性ポリシリコンからなり、ソース領域28aおよびドレイン領域28bはn型シリコンからなっている。このように、ソース領域28aおよびドレイン領域28bを、成膜したn型シリコン膜によって形成しているため、不純物注入工程および活性化工程が不要となり、したがってこれによっても製造工程を簡略化することができる。なお、ソース領域28aおよびドレイン領域28bはn型アモルファスシリコンあるいはn型ポリシリコンからなるものであってもよい。

【0012】次に、図1に示すソース・ドレイン電極形成工程Hにおいて、ソース領域28aおよびドレイン領域28bの各上面等に、クロムからなる第1ソース電極29および第1ドレイン電極30を形成し、続いてその各上面にアルミニウム-チタン合金からなる第2ソース電極31および第2ドレイン電極32を形成する。次に、図1に示すオーバーコート膜成膜工程Iにおいて、全上面にオーバーコート膜33を成膜する。次に、図1に示す水素化工程Jにおいて、水素化用電気炉または水素化用プラズマ炉で水素化処理を行うことにより、チャ

ネル領域27a、ソース領域28aおよびドレイン領域28bのダングリングボンドを減少させる。かくして、ボトムゲート型のポリシリコン薄膜トランジスタが製造される。

【0013】ところで、図1に示す製造工程を、従来のボトムゲート型のポリシリコン薄膜トランジスタの製造工程と比較した場合、脱水素化・ポリ化工程Dおよび水素化工程Jが付加されているだけであるので、従来のボトムゲート型のポリシリコン薄膜トランジスタの製造プロセスラインに脱水素化・ポリ化工程Dのためのエキシマレーザ装置および水素化工程Jのための水素化用電気炉または水素化用プラズマ炉を付加すると、従来のボトムゲート型のポリシリコン薄膜トランジスタの製造プロセスラインを若干変更してそのまま使用することにより、この発明の薄膜トランジスタを製造することができることになる。なお、この発明は、p型のポリシリコン薄膜トランジスタにも適用することができる。

【0014】

【発明の効果】以上説明したように、この発明によれば、水素化アモルファスシリコン膜に、エキシマレーザを前回の照射領域と50%以上オーバーラップさせて照射するスキャン走査によって、脱水素化工程とポリ化工程とを一度に行うことができることとなり、したがって製造工程を簡略化することができ、またこれに伴い設備投資を低減化することができる。

【図面の簡単な説明】

【図1】この発明の一実施形態における薄膜トランジスタの製造工程を示す図。

【図2】(A)～(C)はそれぞれ図1に示す製造工程を経て製造される薄膜トランジスタの各状態における断面図。

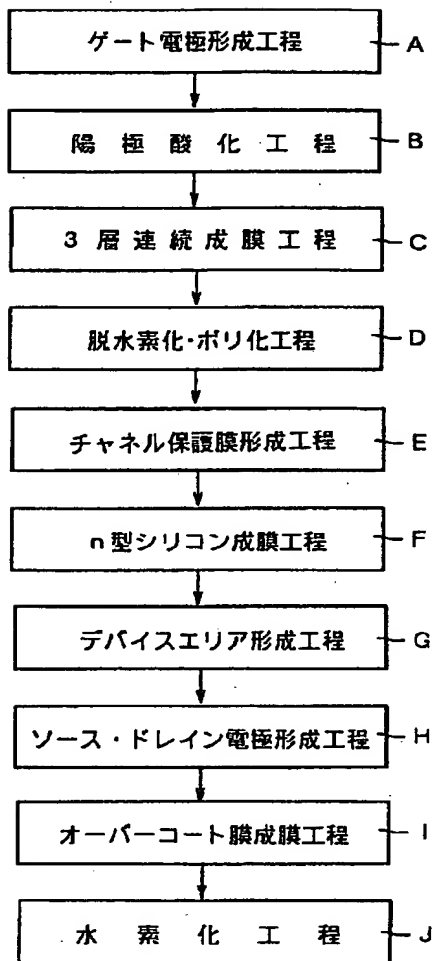
【図3】従来の薄膜トランジスタの製造工程を示す図。

【図4】(A)～(D)はそれぞれ図3に示す製造工程を経て製造される薄膜トランジスタの各状態における断面図。

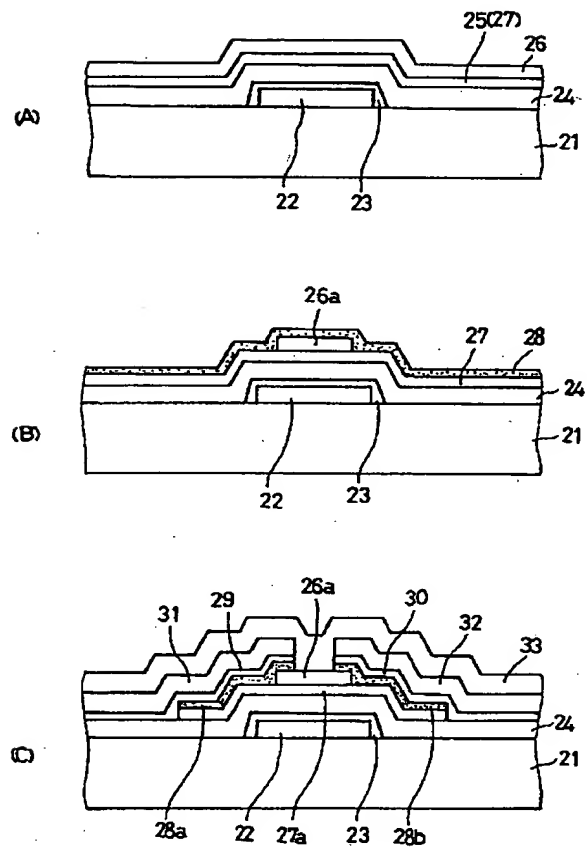
【符号の説明】

- 22 ゲート電極
- 23 第1ゲート絶縁膜
- 24 第2ゲート絶縁膜
- 25 アモルファスシリコン薄膜
- 26 チャネル保護膜形成用膜
- 26a チャネル保護膜
- 27 ポリシリコン薄膜
- 27a チャネル領域
- 28 n型シリコン膜
- 28a ソース領域
- 28b ドレイン領域
- 29 第1ソース電極
- 30 第1ドレイン電極
- 31 第2ソース電極
- 32 第2ドレイン電極

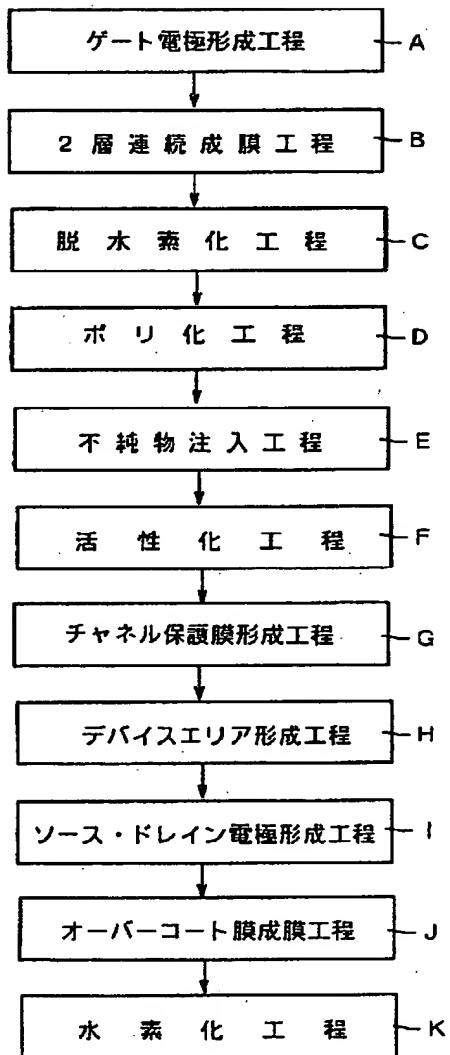
【図1】



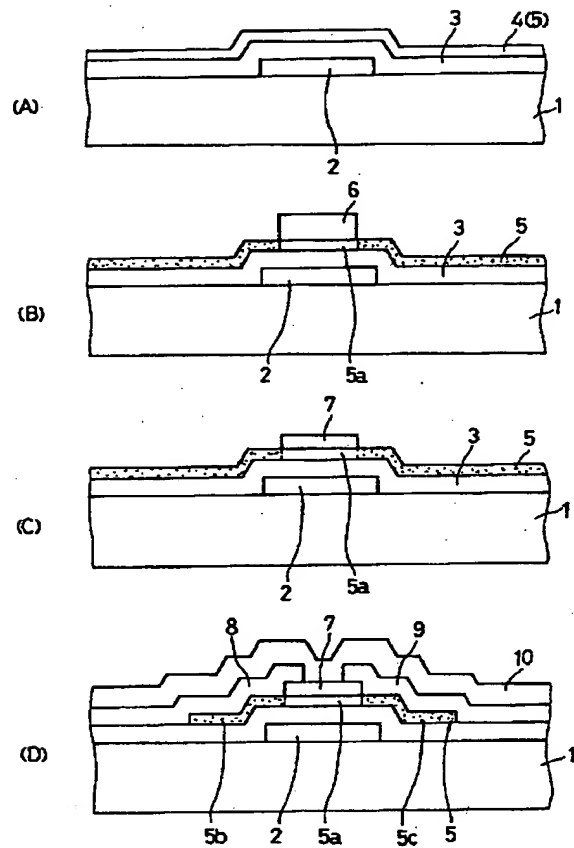
【図2】



【図3】



【図4】



PATENT ABSTRACTS OF JAPAN

(11)Publication number : 09-186336

(43)Date of publication of application : 15.07.1997

(51)Int.Cl.

H01L 29/786

H01L 21/336

(21)Application number : 07-351234

(71)Applicant : CASIO COMPUT CO LTD

(22)Date of filing : 27.12.1995

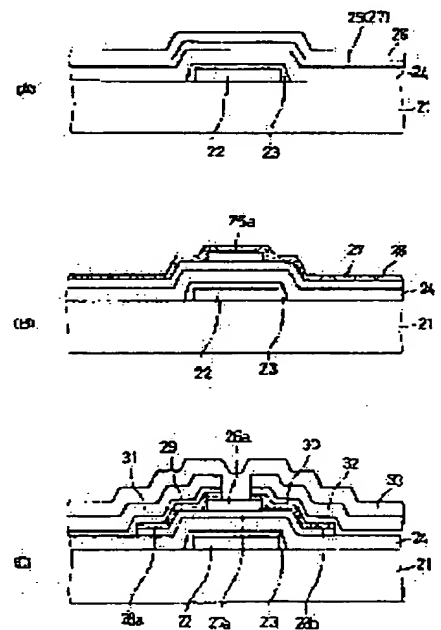
(72)Inventor : KUDO TOSHIO
WAKAI HARUO

(54) METHOD OF MANUFACTURING THIN FILM TRANSISTOR

(57)Abstract:

PROBLEM TO BE SOLVED: To simplify the bottom gate type polysilicon thin film transistor.

SOLUTION: A hydrogen containing true amorphous silicon thin film 25 and a channel protective film forming film 26 comprising a silicon nitride are continuously formed on the surface of the second insulating film 24. Next, the amorphous silicon film 25 is dehydrogenated by irradiating the film 25 with excimer laser in low density in the atmosphere and then the true amorphous silicon thin film 25 is polymerized to form a true polysilicon thin film 27. At this time, this step can be performed simply by changing the energy density of the excimer laser. Besides, after the formation of a channel protective film 26a, a source region 28a and a drain region 28b are formed of a formed n type silicon film. In such a case, both impurity implanting step and activating step can be eliminated.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

*** NOTICES ***

Japan Patent Office is not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

CLAIMS

[Claim]

[Claim 1] The manufacture technique of the TFT which goes the scanning scanning which an excimer laser is made to overlap the last irradiation field 50% or more, and irradiates it at a hydrogenation amorphous silicon layer to all fields, and is characterized for the aforementioned hydrogenation amorphous silicon layer by dehydrogenation-ization and Pori-izing in the manufacture technique of the TFT which uses as an activity semiconductor layer contest polysilicon which has the source, a drain, and a channel field.

[Claim 2] The manufacture technique of the TFT characterized by making an excimer laser overlap last time 90% or more in invention of claim 1 publication.

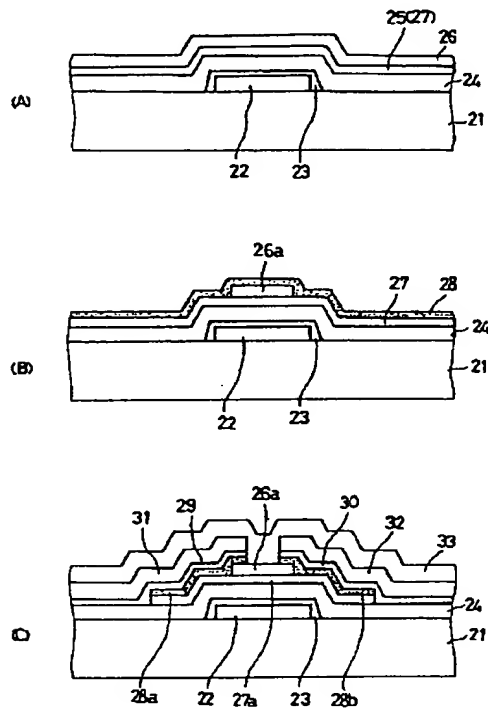
[Claim 3] The manufacture technique of the TFT which makes an excimer laser the long and slender band-like shape of beam which has short width of face in invention of claim 1 publication, and is characterized by carrying out a scanning scanning crosswise [of this band-like beam].

[Claim 4] The manufacture technique of the TFT characterized by carrying out a scanning scanning in invention of claim 1 publication after carrying out multiple-times irradiation of the excimer laser.

[Claim 5] Irradiation of the excimer laser of the aforementioned multiple times is the manufacture technique of TFT that it is characterized by the beginning of an energy density being the lowest in invention of claim 4 publication.

[Claim 6] The manufacture technique of the TFT which makes all fields larger in an energy density than the 1st time after a scanning scanning, and is characterized by carrying out a scanning scanning, irradiating an excimer laser again in invention of claim 1 publication.

[Translation done.]



[Translation done.]

[Kind of final disposal of application other than
the examiner's decision of rejection or
application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's
decision of rejection]

[Date of requesting appeal against examiner's
decision of rejection]

[Date of extinction of right]

Copyright (C); 1998,2000 Japan Patent Office

*** NOTICES ***

Japan Patent Office is not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed description]

[0001]

[The technical field to which invention belongs] This invention relates to the manufacture technique of bottom gate type polysilicon contest TFT especially about the manufacture technique of TFT.

[0002]

[Prior art] Drawing 3 shows the manufacturing process of conventional bottom gate type polysilicon contest TFT, and drawing 4 (A) - (D) shows the cross section in each status of the TFT manufactured through the manufacturing process shown in drawing 3, respectively. In case of a manufacture of this TFT, in gate electrode formation process A first shown in drawing 3, as shown in drawing 4 (A), the gate electrode 2 is formed in the predetermined part of the top of a glass substrate 1. Next, in two-layer continuity **** process B shown in drawing 3, the gate insulator layer 3 and the genuineness hydrogen inclusion amorphous silicon thin film 4 are continued and ****ed on the whole top of the glass substrate 1 containing the gate electrode 2. Next, in dehydrogenation-ized process C shown in drawing 3, when a high energy is given by excimer laser irradiation at a next process, in order to avoid that hydrogen bumps and a defect arises, the hydrogen concentration in the amorphous silicon thin film 4 is reduced by heat-treating with the electric furnace for dehydrogenation-izing.

[0003] Next, in Pori-ized process D shown drawing 3, by irradiating an excimer laser by the high-energy density, the genuineness amorphous silicon thin film 4 is Pori-ized, and the genuineness polysilicon contest thin film 5 is formed. Next, in impurity injection process E shown in drawing 3, as shown in drawing 4 (B), the impurity injection mask 6 is formed on the field which serves as channel field 5a among the polysilicon contest thin films 5, and n type impurities, such as Lynn, are poured into all the fields except channel field 5a among the polysilicon contest thin films 5. Then, the impurity injection mask 6 is exfoliated. Next, in activation process F shown in drawing 3, n type impurity injection field is activated by irradiating an excimer laser by the low-energy density. Next, in channel protective coat formation process G shown in drawing 3, as shown in drawing 4 (C), the channel protective coat 7 is formed on the field which serves as channel field 5a among the polysilicon contest thin films 5.

[0004] Next, in device area formation process H shown in drawing 3, as shown in drawing 4 (D), an unnecessary fraction is removed among the polysilicon contest thin films 5. In this status, the center section of the polysilicon contest thin film 5 is set to channel field 5a which consists of an intrinsic region, and the both sides are set to source field 5b and drain field 5c which consist of an n type impurity injection field. Next, in source drain electrode formation process I shown in drawing 3, the source electrode 8 and the drain electrode 9 are formed in each top of the top both sides of the channel protective coat 7 and source field 5b, and drain field 5c etc. Next, in overcoat ***** process J shown in drawing 3, the overcoat layer 10 is ****ed on all the top. Next, in hydrogenation process K shown in drawing 3, the dangling bond of the polysilicon contest thin film 5 is decreased by performing a hydrogen treating by the electric furnace for hydrogenation, or the plasma furnace for hydrogenation. In this way, bottom gate type polysilicon contest TFT is manufactured.

[Object of the Invention]

[0005] By the way, by the manufacture technique of such conventional bottom gate type polysilicon contest TFT, it is got blocked, dehydrogenation-ized process C, Pori-ized process D, impurity injection process E, activation process F, and hydrogenation process K are added as compared with the manufacture technique of bottom gate type amorphous silicon TFT, and there was a problem with the former of the same type that a manufacturing process was complicated. In this case, especially, since the excimer laser equipment for the electric furnace for dehydrogenation-izing for dehydrogenation-ized process C, Pori-ized process D, and activation process F is separate equipment, it is the factor in which a manufacturing process becomes complicated and equipment investment increases. The technical problem of this invention is reduction-izing equipment investment while it simplifies a manufacturing process.

[0006]

[The means for solving a technical problem] the scanning scanning which this invention makes a hydrogenation amorphous silicon layer overlap an excimer laser 50% or more with the last irradiation field in the manufacture technique of the TFT which uses as an activity semiconductor layer contest polysilicon which has the source, a drain, and a channel field, and is irradiated -- all fields -- going -- the aforementioned hydrogenation amorphous silicon layer -- dehydrogenation-izing -- and it is [Pori-] made toize

[0007] According to this invention, by the scanning scanning which an excimer laser is made to overlap the last irradiation field 50% or more, and irradiates a hydrogenation amorphous silicon layer, a dehydrogenation-ized process and the Pori-ized process can be performed at once, a manufacturing process can be simplified, and equipment investment can be reduction-ized in connection with this.

[0008]

[Gestalt of implementation of invention] Drawing 1 shows the manufacturing process of the bottom gate type polysilicon contest TFT in the 1 enforcement gestalt of this invention, and drawing 2 (A) - (C) shows the cross section in each status of the TFT manufactured through the manufacturing process shown in drawing 1, respectively. In case of a manufacture of this TFT, as gate electrode formation process A first shown in drawing 1 is shown in drawing 2 (A), the gate electrode 22 which consists of an aluminum-titanium alloy is formed in the predetermined part of the top of a glass substrate 21. Next, in anodic oxidation process B shown in drawing 1, the 1st gate insulator layer 23 which consists of an aluminum oxide is formed in the front face of the gate electrode 22 by performing an anodizing. Next, in three layer continuity **** process C shown in drawing 1, the layer for channel protective coat formation 26 which consists of the 2nd gate insulator layer 24, the genuineness hydrogen inclusion amorphous silicon thin film 25, and silicon nitride which consist of a silicon nitride is continuously ****ed by PE-CVD on the whole top of the glass substrate 21 containing the 1st gate insulator layer 23.

[0009] Next, although dehydrogenation-izing and Pori-ized process D shown in drawing 1 are explained, since the layer for channel protective coat formation 26 is ****ed on the intrinsic amorphous silicon thin film 25 of hydrogen inclusion in this case, irradiation of the excimer laser of a low-energy density can perform dehydrogenation-ized processing of the intrinsic amorphous silicon thin film 25 of hydrogen inclusion into the atmospheric air. Then, if an excimer laser is first irradiated in about two 60-150mJ/cm with a low-energy density into the atmospheric air, the hydrogen concentration in the amorphous silicon thin film 25 will decrease, if an excimer laser is subsequently irradiated in about two 150-300mJ/cm with a high-energy density into the atmospheric air similarly, the genuineness amorphous silicon thin film 25 will Pori-ize, and the genuineness polysilicon contest thin film 27 will be formed. Thus, since a dehydrogenation-ized process and the Pori-ized process can be continuously performed only by changing the energy density of an excimer laser, a manufacturing process can be simplified.

[0010] By the way, irradiation of the excimer laser in dehydrogenation-izing and Pori-ized process D is performed by carrying out scanning irradiation, making the long and slender laser beam which has short width of face for a beam size and which was made beltlike overlap crosswise [of a beam size]. In this case, it is important to make the amount of overlap into 90 - 99% more preferably 50% or more.

Moreover, irradiation of an excimer laser makes a low-energy density to an energy density high to **** preferably twice or more, for example, makes a low-energy density and a high-energy density high 2- about 10-20mJ/cm at a time, and it may be made to perform it 3 times or more. There is the technique of enlarging an energy density after covering all fields by the technique of covering all fields in the scan- scanning which shifts so that this 1 after making [in / one field / as the technique of a scanning scanning] an energy density gradually high and irradiating a multiple-times excimer laser field may be overlapped 50% or more, and irradiates an excimer laser, and repeating, and scanning scanning and irradiating an excimer laser by the low-energy density, and irradiating an excimer laser to all fields again. In addition, you may be made to perform lamp irradiation instead of excimer laser irradiation.

[0011] Next, in channel protective coat formation process E shown in drawing 1, as shown in drawing 2 (B), channel protective coat 26a is formed in the predetermined part on the polysilicon contest thin film 27 by removing an unnecessary fraction among the layers for channel protective coat formation 26. Next, in n type silicon **** process F shown in drawing 1, n type silicon layer 28 by which Lynn etc. was doped by the whole top of the polysilicon contest thin film 27 containing channel protective coat 26a by PE-CVD is ****ed. Next, in device area formation process G shown in drawing 1, as shown in drawing 2 (C), while an unnecessary fraction is removed among n type silicon layers 28 and source field 28a and drain field 28b are formed, an unnecessary fraction is removed among the polysilicon contest thin films 27, and channel field 27a is formed. That is, source field 28a and drain field 28b are formed in the top both sides of channel protective coat 26a, and each top of channel field 27a in the both sides. In this case, channel field 27a consists of contest intrinsic polysilicon, and source field 28a and drain field 28b consist of n type silicon. Thus, since source field 28a and drain field 28b are formed with n type silicon layer which ****ed, an impurity injection process and an activation process become unnecessary, therefore a manufacturing process can be simplified also by this. In addition, source field 28a and drain field 28b may consist of an n type amorphous silicon or contest n type polysilicon.

[0012] the [next, / the 1st source electrode 29 which becomes each top of source field 28a and drain field 28b etc. from chromium in source drain electrode formation process H shown in drawing 1, and] - the [the 2nd source electrode 31 which forms 1 drain electrode 30, and becomes each of that top from an aluminum-titanium alloy continuously, and] - 2 drain electrode 32 is formed Next, in overcoat ***** process I shown in drawing 1, the overcoat layer 33 is ****ed on all the top. Next, in hydrogenation process J shown in drawing 1, the dangling bond of channel field 27a, source field 28a, and drain field 28b is decreased by performing a hydrogen treating by the electric furnace for hydrogenation, or the plasma furnace for hydrogenation. In this way, bottom gate type polysilicon contest TFT is manufactured.

[0013] by the way, when the manufacturing process shown in drawing 1 is compared with the manufacturing process of conventional bottom gate type polysilicon contest TFT, [that dehydrogenation-izing, Pori-ized process D, and hydrogenation process J are only added and] If the electric furnace for hydrogenation or the plasma furnace for hydrogenation for the excimer laser equipment for dehydrogenation-izing and Pori-ized process D and hydrogenation process J is added to the manufacture process line of conventional bottom gate type polysilicon contest TFT The TFT of this invention can be manufactured by changing the manufacture process line of conventional bottom gate type polysilicon contest TFT a little, and using it as it is. In addition, this invention is applicable also to p type polysilicon contest TFT.

[0014] [Effect of the invention] As explained above, according to this invention, by the scanning scanning which an excimer laser is made to overlap the last irradiation field 50% or more, and irradiates a hydrogenation amorphous silicon layer, a dehydrogenation-ized process and the Pori-ized process can be performed at once; a manufacturing process can be simplified; and equipment investment can be reduction-ized in connection with this.

[Translation done.]

*** NOTICES ***

Japan Patent Office is not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

TECHNICAL FIELD

[The technical field to which invention belongs] This invention relates to the manufacture technique of bottom gate type polysilicon contest TFT especially about the manufacture technique of TFT.

[Translation done.]

* NOTICES *

Japan Patent Office is not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

PRIOR ART

[Prior art] Drawing 3 shows the manufacturing process of conventional bottom gate type polysilicon contest TFT, and drawing 4 (A) - (D) shows the cross section in each status of the TFT manufactured through the manufacturing process shown in drawing 3, respectively. In case of a manufacture of this TFT, in gate electrode formation process A first shown in drawing 3, as shown in drawing 4 (A), the gate electrode 2 is formed in the predetermined part of the top of a glass substrate 1. Next, in two-layer continuity **** process B shown in drawing 3, the gate insulator layer 3 and the genuineness hydrogen inclusion amorphous silicon thin film 4 are continued and ****ed on the whole top of the glass substrate 1 containing the gate electrode 2. Next, in dehydrogenation-ized process C shown in drawing 3, when a high energy is given by excimer laser irradiation at a next process, in order to avoid that hydrogen bumps and a defect arises, the hydrogen concentration in the amorphous silicon thin film 4 is reduced by heat-treating with the electric furnace for dehydrogenation-izing.

[0003] Next, in Pori-ized process D shown drawing 3, by irradiating an excimer laser by the high-energy density, the genuineness amorphous silicon thin film 4 is Pori-ized, and the genuineness polysilicon contest thin film 5 is formed. Next, in impurity injection process E shown in drawing 3, as shown in drawing 4 (B), the impurity injection mask 6 is formed on the field which serves as channel field 5a among the polysilicon contest thin films 5, and n type impurities, such as Lynn, are poured into all the fields except channel field 5a among the polysilicon contest thin films 5. Then, the impurity injection mask 6 is exfoliated. Next, in activation process F shown in drawing 3, n type impurity injection field is activated by irradiating an excimer laser by the low-energy density. Next, in channel protective coat formation process G shown in drawing 3, as shown in drawing 4 (C), the channel protective coat 7 is formed on the field which serves as channel field 5a among the polysilicon contest thin films 5.

[0004] Next, in device area formation process H shown in drawing 3, as shown in drawing 4 (D), an unnecessary fraction is removed among the polysilicon contest thin films 5. In this status, the center section of the polysilicon contest thin film 5 is set to channel field 5a which consists of an intrinsic region, and the both sides are set to source field 5b and drain field 5c which consist of an n type impurity injection field. Next, in source drain electrode formation process I shown in drawing 3, the source electrode 8 and the drain electrode 9 are formed in each top of the top both sides of the channel protective coat 7 and source field 5b, and drain field 5c etc. Next, in overcoat ***** process J shown in drawing 3, the overcoat layer 10 is ****ed on all the top. Next, in hydrogenation process K shown in drawing 3, the dangling bond of the polysilicon contest thin film 5 is decreased by performing a hydrogen treating by the electric furnace for hydrogenation, or the plasma furnace for hydrogenation. In this way, bottom gate type polysilicon contest TFT is manufactured.

[Translation done.]

*** NOTICES ***

Japan Patent Office is not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

EFFECT OF THE INVENTION

[Effect of the invention] As explained above, according to this invention, by the scanning scanning which an excimer laser is made to overlap the last irradiation field 50% or more, and irradiates a hydrogenation amorphous silicon layer, a dehydrogenation-ized process and the Pori-ized process can be performed at once, a manufacturing process can be simplified, and equipment investment can be reduction-ized in connection with this.

[Translation done.]